AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [1024] with the following amended paragraph:

[1024] Figure 1 depicts an exemplary processor with execution displacement alias prediction encodings. In Figure 1, a processor 107 includes an operation rename unit 101 and a data hazard detection module 103. The data hazard detection module 103, as previously discussed, includes structures utilized to detect a data hazard. Particular implementations of a data hazard detection module include a memory disambiguation buffer (MDB), Load Store Queue (LSQ), etc. However, the described invention is not limited to particular implementations for detecting data hazards, and it should be understood that various realizations of the invention detect data hazards differently (e.g., a single unit that includes multiple stores and logic, separate units that collectively detect data hazards, software emulation, etc.). The operation rename unit 101 includes an aliased read operation encoding 105, an aliased write operation encoding 111, and an alias prediction register bypass encoding 113. The encodings 105, 111, and 113 may be implemented differently in various realizations of the invention (e.g., hardware tables, data structures, a single encoding with multiple access points, etc.). The collection of encodings (whether implemented as a single encoding or plural encoding) and logic associated therewith, may be referred to as an alias predictor. The aliased read operation encoding ~~103~~ 105 identifies read operations that have been detected as aliased and an execution displacement for the identified read operation and corresponding write operation. The aliased read operation encoding may also include additional information to track repetition of alias detection of an identified read operation (e.g., a confidence indicator, a valid bit, etc.). The aliased write operation 111 identifies write operations that have been detected as aliased. The alias prediction register bypass encoding 113 identifies a potential aliasing write operation and its renamed register. The alias prediction register bypass encoding 113 may also track the number of predictions made for each indicated write operation.

Please replace paragraph [1062] with the following amended paragraph:

[1062] Figure 7 depicts exemplary processor blocks that predict aliasing and verify predicted aliasing. An operation rename unit 701 is coupled with an operation scheduling unit 703, load store queue (LSQ) 705, and an operation retirement unit 707. Although the exemplary processor illustrated in Figure 7 includes load store queue, realizations may include other data hazard detection units, such as a memory disambiguation buffer. Various realizations of the invention may include fewer or additional components not illustrated in Figure 7. For example, the operation renaming unit may be preceded by one or more components that fetch and decode operations. The operation rename unit 701 issues operations to the operation scheduling unit 703. The operation scheduling unit 703 schedules and passes memory operations to the LSQ 705. The LSQ ~~705sends~~ 705 sends re-issue signals to the operation scheduling unit 703 if necessary. The LSQ 705 sends alias detection signals, which indicate write and read operation information, and misprediction signals that identify the relevant read operation to the operation rename unit 701. The LSQ ~~705also~~ 705 also sends flush signals to the operation retirement unit 707. The operation retirement unit 707 provides a write retire query to determine if a corresponding predicted to alias read operation counter is equal to zero. In another example, the operation renaming unit 701 sends signals to the operation retirement unit 707 to indicate when a write operation can be retired in accordance with the corresponding predicted to alias read operation counter.

Please replace paragraph [1063] with the following amended paragraph:

[1063] The described invention may be provided as a computer program product, or software, that may include a machine-readable medium having stored thereon instructions, which may be used to program a computer system (or other electronic devices) to perform a process according to the present invention. A machine readable medium includes any mechanism for storing or transmitting information in a form (e.g., software, processing application) readable by a machine (e.g., a computer). The machine-readable medium may include, but is not limited to, machine-readable storage mediums and machine-readable transmission mediums. The machine-readable storage medium may include, but is not limited to, magnetic storage medium (e.g., floppy diskette); optical storage medium (e.g., CD-ROM); magneto-optical storage medium; read only memory (ROM); random access memory (RAM); erasable programmable memory (e.g., EPROM and EEPROM); and flash memory; or other types of medium suitable for storing

electronic instructions. The machine-readable transmission medium may include, but is not limited to, electrical, optical, acoustical or other form of propagated signal (e.g., carrier waves, infrared signals, digital signals, etc.)~~; or other types of medium suitable for storing electronic instructions~~.